Amendments to the Drawings:

The attached sheet of drawings includes changes to Figure 2. This sheet, which includes Figure 2, replaces the original sheet including Figure 2.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

In the Office action dated May 12, 2005, the following objections and rejections were made. Figure 2 was objected to. The specification was objected as failing to provide proper antecedent basis for claims 9 - 36. Claims 1 - 44 were rejected under 35 U.S.C. § 112, first paragraph. Claims 1 and 37 were rejected under 35 U.S.C. § 102. Claims 5, 8, 41 and 44 were rejected under 35 U.S.C. § 103. Claims 9 - 36 were not examined. Claims 2 - 4, 6, 7, 38 - 40, 42 and 43 were objected to but were deemed allowable if rewritten to overcome the rejection(s) under 35 U.S.C. § 112, and rewritten to include all of the limitations of the base claim and any intervening claims.

By this Amendment, Applicant has amended claims 1, 3, 6, 9, 11, 12, 17, 19, 21, 25, 27, 28, 31, 33, 35, 37, 39 and 42 and canceled claims 2, 20, 34 and 38. Reconsideration and reexamination are hereby requested for claims 1, 3 - 19, 21 - 33, 35 - 37 and 39 - 44 that are now pending in this application.

Response to the Objection to the Drawings

The Examiner requested that Figure 2 be designated as prior art. Applicant has amended Figure 2 as requested.

Response to the Objection to the Specification

The Examiner objected to the specification as failing to provide proper antecedent basis for the claimed subject matter under 37 C.F.R. 1.75(d)(1) and MPEP §60801(o). Specifically, the Office action states "claims 9 - 36 were directed to

circuits for performing a line loop back test starting from a serializer to a first-in-first-out buffer to a loop back data multiplexer, and then a deserializer which is contradictory to the claimed invention as disclosed in the specification disclosure which is directed to a circuit for performing a line loop back test starting from a deserializer to a loop back multiplexer, to a first-in-first-out buffer, and then a serializer." (Underlining added by Applicant.)

Applicant respectfully traverses this objection. Initially, any terminology set forth in the quotation above (e.g., "a line loop back test starting from . . . ") that does not appear in the claims is not part of the claim and, as such, cannot form a proper basis for rejecting the claims.

Applicant assumes that the Examiner is objecting to the order in which the elements of the claims are set forth. Implicit here is an assumption that this order must limit the claims in some manner. However, Applicant notes that claims 9 - 36 are directed to circuits and, according to conventional practice, the claims set forth how those circuits are interconnected. There is no requirement to Applicant's knowledge in the MPEP or anywhere else that requires that the elements of an apparatus be set forth in any particular order.

Moreover, read in their entirely, the claims are entirely consistent with the specification. In particular, the wherein clauses in each independent claim recite how elements of the claims are coupled. Taking claim 9 as an example:

wherein the deserializer parallel data output signal is coupled to the loop back data buffer parallel input signal;

wherein the loop back data buffer parallel output signal is coupled to the loop back data multiplexer parallel loop back input signal;

wherein the loop back data multiplexer parallel data output signal is coupled to the FIFO parallel data input signal;

wherein the FIFO parallel data output signal is coupled to the serializer parallel data input signal.

A comparison of the above terms with, for example, the components of Figures 3 and 4 shows that the specification and claims are entirely consistent. In view of the above, Applicant submits that the specification and claims 9 - 36 are in proper form. Accordingly, Applicant submits that this rejection should be withdrawn.

Response to the 35 U.S.C. § 112 Rejection of the Claims

Claims 1 - 44 were rejected under 35 U.S.C. § 112, first paragraph, as based on a disclosure which is not enabling. In particular, the Office states that the "features of method and circuitry for performing a line loop back test in line loop back mode are critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure" citing *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Applicant respectfully traverses this rejection because the rule set forth in *In re Mayhew* is inapplicable to this application. In *In re Mayhew* the rejection was based on the grounds that "applicant has disclosed that--cooling a portion of the molten spelter . . . --are essential steps in his inventive process." 527 F.2d at 1232 (Underlining added). For example, the case indicated that that the specification set forth "two criteria. First, iron must be alloyed with zinc out of contact with an oxidizing atmosphere. . . . Second, the main body of the spelter bath is kept at a temperature higher that that which is ordinarily considered optimum." 527 F.2d at 1232-33 (Underlining added).

In contrast, Applicant's specification does not state that the features cited by the Examiner are "essential" or that any particular feature or method "must be" performed. In fact, Applicant's specification teaches that many features may not be required. See, for example, the specification at page 11, lines 26 - 31 that states:

> While the present invention has been described with reference to its preferred and alternative embodiments, those embodiments are offered by way of example, not by way of limitation. Those skilled in the art will be enabled by this disclosure to make various additions, deletions, and modifications to the present invention. Accordingly, all such additions, deletions, and modifications are deemed to lie within the spirit and scope of the present invention as delineated in the appended claims.

Finally, it is well established that the original claims form a part of the disclosure. Accordingly, Applicant's original claims also serve to disclose, for purposes of 35 U.S.C § 112, the combinations of elements and steps recited in claims 1 - 44.

In view of the above, Applicant submits that claims 1 - 44 are adequately supported by the specification. Accordingly, Applicant submits that this rejection should be withdrawn.

Response to the 35 U.S.C. § 102 Rejection of the Claims

The Examiner rejected claims 1 and 37 under 35 U.S.C. § 102(e) as being unpatentable over Ducaroir et al., U.S. Patent Application Publication No. 2001/0043648 (hereafter referred to as "Ducaroir").

Claims 1 and 37 have been amended as set forth above. Applicant submits that the amended claims are patentable over the references of record.

Response to the 35 U.S.C. § 103 Rejections of the Claims

The Examiner rejected claims 5, 8, 41 and 44 under 35 U.S.C. § 103(a) as being unpatentable over Ducaroir in view of Ramamurthy et al., U.S. Patent No. 5,787,114 (hereafter referred to as "Ramamurthy"). Claims 5 and 8 depend on independent claim 1. Claims 41 and 44 depend on independent claim 37.

As stated at paragraph 7 on page 5 of the Office action, the rejection of these claims is based on Ramamurthy that "teaches the uses of a low speed parallel loop back buffer (16) that provides coupling between the deserializer and the low

speed parallel loop back data multiplexer and a clock and data recovery unit (17) that provide coupling between the receiver and the deserializer."

Applicant notes, however, that as shown in Figure 3 of Ramamurthy, the input buffer is coupled between the serial input 7 and the deserializer 12. Accordingly, Ramamurty does not teach or suggest the use of "a low speed parallel loop back data buffer" that "provides coupling between" a "deserializer" and a "low speed parallel loop back data multiplexer" as claimed in claims 5 and 41.

In addition, Ramamurty discloses that the data and clock recovery unit 17 operates on the output of the deserializer 12. Thus, Ramamurty does not teach or suggest the use of a "clock and data recovery unit" that "provides coupling between" a "receiver" and a "deserializer" as claimed in claims 8 and 44.

In view of the above, Applicant submits that claims 5, 8, 41 and 44 are not obvious in view of the cited references.

Claim 9 - 36

Independent claims 9, 17, 25 and 31 have been amended as set forth above. Applicant submits that amended claims 9, 17, 25 and 31 are patentable over the cited references.

The dependent claims that depend on the independent claims discussed above also are patentable over the cited references for the reasons set forth above. In addition, these dependent claims are patentable over these references for the additional limitations that these claims contain.

CONCLUSION

For the foregoing reasons Applicant submits that the claims are patentable over the references of record. Reexamination and reconsideration are respectfully requested.

Respectfully submitted,
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SDB/vsj

APPENDIX